CS-03-021

January 5, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/688,047 10/17/03

Chung Foong Tan et al.

END OF RANGE (EOR) SECONDARY DEFECT ENGINEERING USING SUBSTITUTIONAL CARBON DOPING

INFORMATION DISCLOSURE STATEMENT

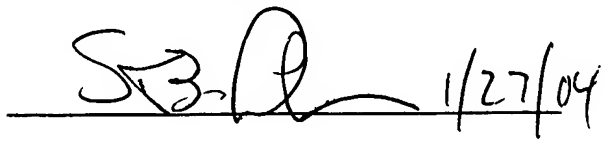
Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date  1/27/04

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In the article "Optimum Halo Structure for Sub-0.1um CMOSFETs", Wen-Kuan Yeh et al., IEEE Transaction on Electron Deivces, Vol. 48, No. 10, October 2001, pp. 2357-2362, optimized halo structures for sub-0.1um CMOS-FETs are evaluated.

In the article "Antimony Assisted Arsenic S/D Extension Engineering for Sub-0.1um nMOSFETs: A Novel Approach to Steep and Retrograde Indium Pocket Profiles," Howard C.H. Wang et al., IEDM 2001, proposes a novel process whereby Antimony Assisted Arsenic S/D Extension is employed to realize a steep and retrograde indium pocket profile for sub-0.1um nNOSFETs.

In the article "Effects of end-of-range dislocation loops on transient enhanced diffusion of indium implanted in silicon," T. Noda et al., Journal of Applied Physics, Vol. 88, No. 9, November 2001, pp. 4980-4984, transient enhanced diffusion of indium implanted in silicon is studied in the presence of the end-of-range (EOR) damage layer.

The article "Enhanced electrical activation of indium coimplanted with carbon in a silicon substrate," H. Boudinov et al., Journal of Applied Physics, Vol. 86, No. 10, pp. 5909-5911, November 15, 1999, discusses low dopant activation.

The articles "Indium transient enhanced diffusion," P.B. Griffin et al., Applied Physics Letters, Vol. 73, No. 20, pp. 2986-2988, Nov. 16, 1998, and "Evolution of end-of-range damage and transient enhanced diffusion of indium in silicon," T. Noda, Journal of Applied Physics, Vol. 91, No. 2, pp. 639-645, Jan 15, 2002, discuss transient enhanced diffusion (TED).

Reports have shown that with the incorporation of carbon into the amorphous-crystalline silicon interface of the dopant implant profile, EOR secondary defects can be removed. This interface is an area or region at the tail end of the implant profile which maintains its crystalline property, but it is saturated with the dopant impurity. This is discussed in the articles "Elimination of secondary defects in preamorphized Si by C+ implantation," Satoshi Mishikawa et al., Applied Physics Letters, 62(3), Jan. 18, 1993, pp. 303-305 and "Removal of end of range defect in Ge+ pre-amorphized Si by carbon ion implantation," Peng-Shiu Chen et al., Journal of Appled Physics, Vol. 85, No. 6, March 15, 1999, pp. 3114-3119.

"Suppression of dislocation formation in silicon by carbon implantation," T.W. Simpson et al., Applied Physics Letters, 67(19), Nov. 6, 1995,pp. 2857-2859, discusses substitutional carbon was shown to act as a sink for silicon interstitials formed, preventing the clustering of silicon interstitials, thereby preventing EOR secondary defect formation.

U.S. Patent 6,541,829 to Nishinohara et al., "Semiconductor Device and Method of Manufacturing the Same," discloses an indium halo implant.

U.S. Patent 6,514,886 to U'Ren, "Method for Elimination of Contaminants Prior to Epitaxy," teaches an RPCVD method prior to epitaxy.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
CS-03-021	10/688,047
Applicant: Chung Foong Tan et al.	
Filing Date: 10/17/03	Group Art Unit

U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	6541829	4/1/03	Nishinohara et al.	257	402	12/1/00
	6514886	2/4/03	Li'Ren	438	791	9/22/00

FOREIGN PATENT DOCUMENTS

Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- "Optimum Halo Structure for Sub-0.1 μm CMOSFETs", Wen-Kuan Yeh et al., IEEE Trans. on Electron Devices, Vol. 48, No. 10, Oct. 2001, pp. 2357-2362.
- "Antimony Assisted Arsenic S/D Extension Engineering for Sub-0.1μm nMOSFETs: A Novel Approach to Steep and Retrograde Indium Pocket Profiles," Howard C.H. Wang et al., IEDM 2001.

Examiner	Date Considered

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